REMARKS

Claims 1-22 are pending in the application, with Claims 1, 5, 9, and 16 being independent claims. Claims 1-5, 7-17, 21, and 22 are rejected under 35 U.S.C. § 102(b) as being anticipated by Anantharaman et al. (US Patent Publication No. 2002/0093978 A1). In addition, Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Anantharaman et al. (US Patent Publication No. 2002/0093978 A1) in view of Quirk et al. (US Patent No. 5,675,617 A). Also, Claims 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable Anantharaman et al. (US Patent Publication No. 2002/0093978 A1) in view of Park et al. (US Patent No. 6,529,528 B1).

Anantharaman et al. discloses a method of encoding and decoding frames of data used in a synchronous protocol, such as HDLC. The method operates on blocks of data, as opposed to serial bits and uses a first reference ("lookup") table for zero insertion during the data encoding process and a second reference table for flag or abort signal detection and zero deletion during the data decoding process. Since all of the encode procedure requirements are integrated into the first reference table, only a single read operation is required for bit stuffing. On the decode side, since all of the decode procedure requirements are integrated into the second reference table, decoding is performed on bytes of data with a single read of the second table.

Park et al. discloses a multiplexing method for multimedia communication by changing a header of a multiplex protocol data unit. It is respectfully submitted that Park et al. is commonly assigned with present application to Samsung Electronics Co., Ltd., as well as to The Regents of the University of California. Park et al. is not a proper prior art reference under 35 USC §103 (c)(2), as Park et al. appears to have been subject to a joint research agreement, i.e. a written contract, grant or cooperative agreement entered into for the performance of experimental, developmental, or research work in the field of the claimed invention (35 USC §103 (c)(3)).

Quirk et al. discloses a method to encode and to decode frames of data used in synchronous protocols by operating on blocks of data, such as data bytes or data words, in a

parallel rather than a bit serial manner.

The present invention is directed to a method for synchronizing data frames capable of preventing flag emulation without decreasing a processing speed in a communication system. Independent Claim 1 recites, in part, classifying the data sequence into N unit data sequences having a predetermined bit number and inputting an n^{th} unit data sequence to be checked from among the N unit data sequences into a predetermined table as indices; and outputting output data sequences from the table in correspondence to the indices together with at least one attribute. Independent Claim 5 recites, in part, classifying a received data sequence into N unit data sequences having a predetermined bit number; defining at least one attribute of an $n\text{-}1^{th}$ unit data sequence from among the N unit data sequences, the at least one attribute indicating a number of the bit values which are sequentially continued starting from a most significant bit (MSB) of the corresponding unit data sequence; and inputting attributes of an n^{th} unit data sequence and the $n\text{-}1^{th}$ unit data sequence into a table, and outputting attributes of the corresponding output data sequence and the nth unit data sequence. Independent Claim 9 recites classifying the data sequence into a plurality of unit data sequences having a predetermined bit number, and sequentially inputting the unit data sequences into a predetermined table as indices; outputting output data sequences from the table in correspondence to the indices, the output data sequences having dummy bits which are alternatively inserted; and forming the data frame from the output data sequences, and attaching the flags to front and rear ends of the data frame, respectively. Independent Claim 16 recites classifying a received data sequence into a plurality of unit data sequences having a predetermined bit number; and sequentially inputting the unit data sequences into a predetermined table, and sequentially outputting the output data sequences from which the dummy bits are removed from the table in correspondence to the input unit data sequences.

With respect to Claim 1, the Examiner states that at page 2, paragraph 0028 through page 3, paragraph 0039, and Figs. 4 and 5, Anantharaman et al. discloses (a) classifying the data sequence into N unit data sequences having a predetermined bit number and inputting an n^{th} unit data sequence to be checked from among the N unit data sequences into a predetermined table as

indices; and (b) outputting output data sequences from the table in correspondence to the indices together with at least one attribute, the output data sequences having dummy bits (interpreted as stuffed bits) which are alternatively inserted into the unit data sequences the at least one attribute indicating a number of the bit values which are sequentially continued starting from a most significant bit (MSB) of the output data sequence, the indices including an attribute output from the table with respect to an n-1^{th} unit data sequence.

With respect to Claim 5, the Examiner states that at page 2, paragraph 0028 through page 3, paragraph 0039, and Figs. 4 and 5, Anantharaman et al. discloses (a) classifying a received data sequence into N unit data sequences having a predetermined bit number defining at least one attribute of an n-1^{th} unit data sequence from among the N unit data sequences, the at least one attribute indicating a number of the bit values which are sequentially continued starting from a most significant bit (MSB) of the corresponding unit data sequence; and (b) inputting attributes of an n^{th} unit data sequence and the n-1^{th} unit data sequence into a table, and outputting attributes of the corresponding output data sequence and the n^{th} unit data sequence.

With respect to Claim 9, the Examiner states that at page 2, paragraph 0028 through page 3, paragraph 0039, and Figs. 4 and 5, Anantharaman et al. discloses (a) classifying the data sequence into a plurality of unit data sequences having a predetermined bit number, and sequentially inputting the unit data sequences into a predetermined table as indices; (b) discloses outputting output data sequences from the table in correspondence to the indices, the output data sequences having dummy bits which are alternatively inserted, (c) discloses forming the data frame from the output data sequences, and attaching the flags to front and rear ends of the data frame, respectively.

With respect to Claim 16, the Examiner states that at page 2, paragraph 0028 through page 3, paragraph 0039, and Figs. 4 and 5, Anantharaman et al. discloses (a) discloses classifying a received data sequence into a plurality of unit data sequences having a predetermined bit number; (b) discloses sequentially inputting the unit data sequences into a predetermined table, and sequentially outputting the output data sequences from which the dummy bits are removed

from the table in correspondence to the input unit data sequences.

Applicant respectfully submits that the Examiner is in error in the application of Anantharaman et al. because Anantharaman et al. provides substantially two look up tables for encoding and decoding the data. The first reference lookup table provides zero insertion during the data encoding process and the second reference look up table provides flag or abort signal detection and zero deletion during the data decoding process. The claims of the present application provide a single look up table having the encoded dummy bits starting from the most significant bit (MSB), and provide indicator flags for each encoded data sequence. Thereby, the data sequence includes both the dummy bits and flags for encoding and decoding the data bits from a single look up table.

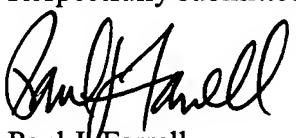
Accordingly, Applicant believes independent Claims 1, 5, 9, and 16 are allowable over Anantharaman et al.

While not conceding the patentability, per se, of dependent Claims 2-4, 7, 8, 10-15, 17, 21, and 22, Applicant believes they are allowable for at least the above-described reasons.

Independent Claims 1, 5, 9 and 16 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 2-4, 6-8, 10-15 and 17-22, these are likewise believed to be allowable by virtue of their dependence on their respective independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 2-4, 6-8, 10-15 and 17-22 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1-22, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,



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